



On comparison of the main electrical properties of Cr/n-type Si and Re/n-type Si metal semiconductor structures

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In our study, the ideality factors, barrier heights and series resistances with main electrical properties of Cr/n-type Si and Re/n-type Si metal semiconductor (MS) structures have been investigated using current-voltage (I - V) measurements. Using forward bias I - V measurements, selected electrical parameters of these MS were obtained and compared at room temperature. The main electrical such as ideality factor (n) and barrier height (Φ_b) of Cr/n-Si and Re/n-Si structures were found as 1.406 and 1.404, and 0.629 eV and 0.696 eV, respectively. Furthermore, ideality factor (n), barrier height (Φ_b) and series resistance (R_s) values were calculated by using Cheung's functions and compared by each other. It was concluded that the main electrical parameters obtained from Cr/n-type Si and Re/n-type Si MS structures are in close agreement with each other.

Keywords: Ideality factor; Barrier height, Series resistance, MS structure

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Introduction

Metal-semiconductor (MS) structures are considerable importance in the development semiconductor device technology. Metal-semiconductor (MS) structures are one of the most widely used rectifying contacts in the electronics industry [1, 2, 5, and 6]. Owing to the technological importance of the metal-semiconductor structures in the electronics industry had been extensively studied both experimental and theoretically. Thus, the metal semiconductor technology is still investigated and has attracted much attention during recent years [1, 2]. Metal-semiconductor structures and devices continue to occupy a preeminent technological position due to their importance when building integrated electronic systems used in a wide range of applications from computers, capacitors, cell-phones, transistors, digital cameras and electronic entertainment systems, to electronic instrumentation for medical diagnostics and environmental monitoring [5-9].

In this study, the main electrical properties such as ideality factors, barrier heights and series resistances of the Cr/n-type Si and Re/n-type Si metal semiconductor (MS) structures investigated using current-voltage (I - V) measurements. Furthermore, we compared the Cr/n-type Si and Re/n-type Si metal semiconductor (MS) according to different parameters and various methods.

Experimental

Experimentally, Cr/n-type Si and Re/n-type Si (1 0 0) structures were prepared with high resistivity on profile of I - V characteristics of them. Before the production process, firstly, n-Si wafer with 1-10 Ω .cm resistivity was subjected to chemical cleaning processes in ammonium-peroxide for 1 min to get rid of native-oxide and organic residuals on the surface. After that, it was cleaned in the $H_2SO_4:H_2O_2:H_2O$ with 3:1:1 and $HCl:H_2O$ with 1:1 volume ratio for 1 min, and then

it was dried by dry nitrogen gas to obstacle any oxidation on the surface. The cleaning procedure can be found in the literature and our previous studies [4, 10-12]. Also, the flow chart of the experimental procedure is given in Fig. 1.

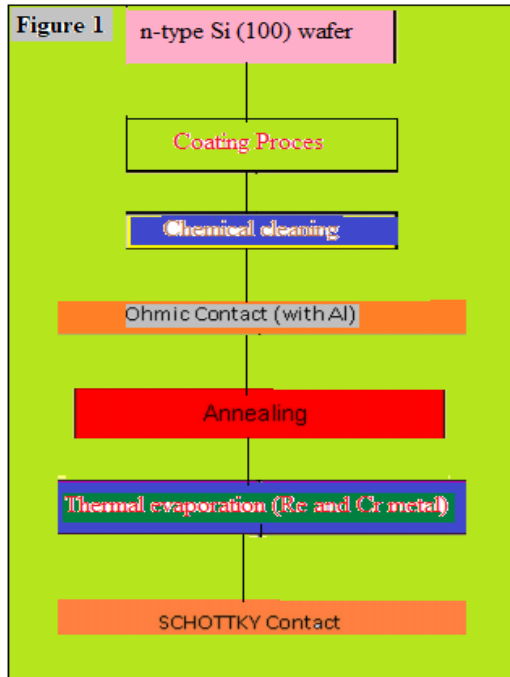


Figure 1. Schematic cleaning diagram of metal semiconductor structures process.

All evaporation processes were carried out in a turbo molecular fitted vacuum coating unit at about 10^{-6} mbar. The current-voltage (I - V) measurements carried out by the use of a Keithly 2400 programmable constant current source.

Results and discussion

The obtained Cr/ n -type Si and Re/ n -type Si structures were characterized by calculating diode parameters from current-voltage (I - V) measurements. The I - V plots of the Cr/ n -type Si and Re/ n -type Si (1 0 0) metal semiconductor structures at temperature are shown in Fig. 2.

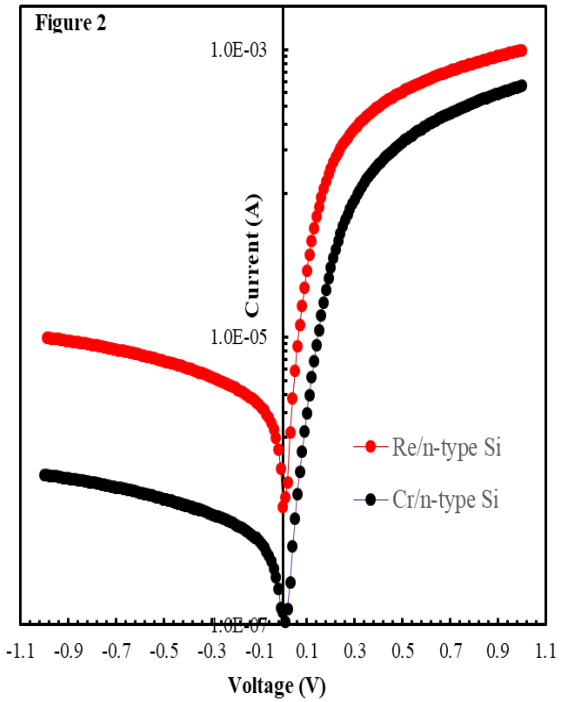


Figure 2. The experimental forward and reverse bias current versus voltage characteristics of Cr/ n -type Si and Re/ n -type Si MS structures at room temperatures.

Thermionic emission (TE) theory was used to determine ideality factors (n) and barrier heights (Φ_b). Thermionic emission current and it can be expressed by [1-7, 14, 15];

$$I = I_o \exp\left(\frac{qV}{nkT}\right) \left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \quad (1)$$

where q is the electron charge, V the forward applied voltage, n the ideality factor, k the Boltzman constant $1.38 \times 10^{-23} \text{ J K}^{-1}$, T the absolute temperature and I_o is the saturation current derived from the straight line intercept of $\ln I$ at $V=0$ and is given by;

$$I_o = AA^* T^2 \exp\left(-\frac{q\Phi_{bo}}{kT}\right) \quad (2)$$

where A is the effective diode area, A^* is the effective Richardson constant of $112 \text{ A cm}^{-2} \text{ K}^{-2}$ for p -type Si [1-4], Φ_{bo} is the zero bias barrier height, respectively. If Eq. (1) and Eq. (2) are reorganized for n and Φ_b , the next equations are obtained:

$$n = \frac{q}{kT} \left(\frac{dV}{d \ln I} \right) \quad (3)$$

And the barrier height Φ_{bo} is determined from the extrapolated I_o and is given by the relation;

$$\Phi_{bo} = \frac{kT}{q} \ln\left(\frac{AA^* T^2}{I_o}\right) \quad (4)$$

Therefore, using Eq. (3) and Eq. (4) the values of the ideality factor and barrier height of the diode at room temperatures were calculated from the slope of the linear region of the forward bias $\ln(I)$ - V plots in Fig. 2, and these values obtained as 1.406 , 1.404, and 0.629, 0.696 eV for of Cr/*n*-type Si and Re/*n*-type Si MS structures, respectively. As can be seen, the experimental ideality factors and barrier heights vary from diode to diode, but the obtained values are in close agreement with each other. The values of ideality factor (for $n > 1$) indicate that the interface oxide layer may be formed either during surface preparation and metal evaporation [1-10].

Another method to determine the main parameters of metal-semiconductor structures is Cheung method. Because, at higher voltages, series resistance becomes significant on MS device behavior. Thus, the values of n , R_s and Φ_b were evaluated using a method developed by Cheung et al.[15]. The Cheung's method is achieved by using the functions;

$$\frac{dV}{d(\ln I)} = n \frac{kT}{q} + R_s I \quad (5)$$

$$H(I) = V - n \left(\frac{kT}{q} \right) \ln \left(\frac{I}{AA^* T^2} \right) \quad (6)$$

and

$$H(I) = IR_s + n\Phi_{bo} \quad (7)$$

Firstly, it is possible to estimate R_s and n by using Eq. 5 and then, by using the obtained n values, it is possible to estimate Φ_b from Eqs. 6 and 7. When the $dV/d(\ln I)$ and $H(I)$ is plotted against to current, a straight line is obtained. The slope and intercept of these two plots provide to determine the R_s , Φ_b and n . Thus, while Fig. 3 display the $dV/d(\ln I)$ - I graphs of the Cr/*n*-type Si and Re/*n*-type Si MS structures,

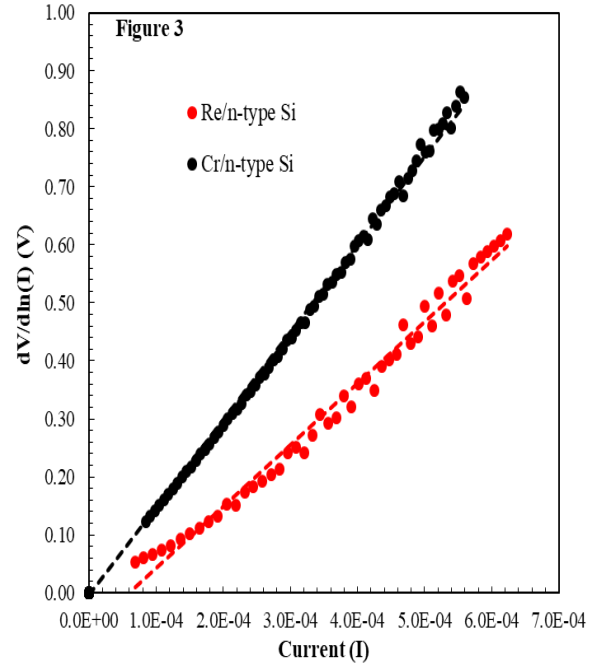


Figure 3. Experimental $dV/d\ln(I)$ vs I curves of Cr/*n*-type Si and Re/*n*-type Si MS structures at room temperatures.

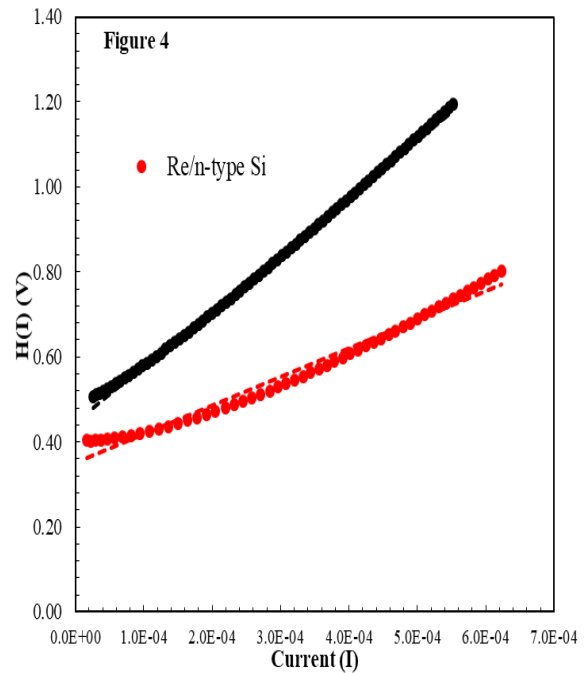


Figure 4. Experimental $H(I)$ vs I curves of Cr/*n*-type Si and Re/*n*-type Si MS structures at room temperatures.

Fig. 4 show $H(I)$ - I plots of Cr/*n*-type Si and Re/*n*-type Si MS structures, respectively. Thus, for Cr/*n*-type Si and Re/*n*-type Si MS structures, the series resistance and ideality factor values were calculated from Fig. 3 using Eq.5 and were found to be 1508 Ω , 1061 Ω and 1.16, 1.267, respectively. Likewise, the series resistance and barrier height values were

calculated from Fig. 4 using Eq. 7 and were found to be 1327 Ω , 680 Ω and 0.384 eV, 0.211 eV, respectively. The differences at the main electrical properties can be attributed to the approximation differences between the thermionic emission theory and Cheung methods.

Conclusion

In this work, we investigated the main electrical characteristic of the Cr/n-type Si and Re/n-type Si MS structures at room temperature I - V measurements. Cr/n-type Si and Re/n-type Si MS structures exhibited a Schottky diode-like behavior at low applied voltages. The main electronic characteristics of these Cr/n-type Si and Re/n-type Si MS structures such as ideality factor, barrier heights and series resistances were calculated from both the Thermionic Emission (TE) theory and Cheung methods and compared each other. The ideality factor values obtained from I - V characteristics are higher than unity, and that is attributed to the presence of a thin interfacial insulator layer between the metal and semiconductor. The experimental result obtained showed that main electrical parameters such as ideality factor, barrier height and series resistance have strong correlation with the applied bias.

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